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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,593	11/28/2003	Pascal Gabet	4590-242	5672

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LOWE HAUPTMAN & BERNER, LLP
1700 DIAGONAL ROAD, SUITE 300
ALEXANDRIA, VA 22314

EXAMINER	
LE, DINH THANH	
ART UNIT	**PAPER NUMBER**
2816	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/722,593	GABET ET AL.	
	Examiner	Art Unit	
	DINH T. LE	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2 and 4-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

NON-FINAL REJECTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/25/2008 has been entered.

The rejection of claims 1-2 and 4-9 and 17 under 35 USC 112, second paragraph, has been withdrawn in the amendments to these claims.

Claim Rejections

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 10-11 and 13-16 are rejected under 35 USC 102 (b) as being anticipated by Pertersson et al (US 5,140,284).

As the best construed, Petersson et al disclose in Figure 2 a circuit comprising:

- a synthesizer (21-25) for synthesizing a frequency (25-1 12.5M1c) with a variable steps (j7.5MlIZ- 25M1'17,=12.5M1V to 112.5M1-12-75M1R=37.5M114, see Table 1 at column 5;
- one variable rank divider (26) having a division number N located after the synthesizer (221-25);

- a divider (26) for dividing the output (fVCO) by a division value P;

- a frequency controller (31) for deliver division rank command to the diver (26) and the frequency command to the divider (25) having a division value (N) for controlling the variable frequency steps; and

- wherein a length of a cycle of evolution of N is variable and dependent on a value of P, see lines 10-36 and Table I, column 5 in which the division N is varied from 1000 to 4000 in corresponding to the change of the division R from 20 to 60.

- With regard to claim 11, the variable-rank divider R is varied according to an arithmetic Sequence, see Table I in column 5.

Claim Rejections - 35 USC § 103

> The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 4-9, 12 and17-20 are rejected under 35 USC 103(a) as being unpatentable over Petersson et al (US 5,140,284) in view and Figure 2 of the applicant's admitted prior art and further in view of Dekker (US 6,239,660).

Petersson et al discloses a synthesizer circuit

As the best construed, Petersson et al disclose in Figure 1 a circuit comprising:

- a synthesizer (21-25) for synthesizing a frequency (25-112.5MHZ) with a variable steps (37.5MHZ- 25MHZ=12.5MHZ to 112.5MHZ-75MHZ=37.5MHZ), see Table 1 at column 5;

- one variable rank divider (26) located after the synthesizer (221-25); and

- a frequency controller (31) for deliver division rank command to the diver (26), the frequency command to the divider (21) for controlling the variable frequency steps and the synthesis command to the divider (25) for controlling the synthesis steps.

However, Petersson et al does not disclose that the synthesizer is a fractional step phase-locked loop synthesizer and a filter is placed after the divider.

The applicant's admitted prior art teaches in Figure 2 a synthesizer comprising a fractional step modulo for providing fractional frequency steps.

Dekker teaches in Figure 2 a synthesizer circuit comprising a filter (212) placed after the synthesizer (200) for removing unwanted high frequency noise.

It would have been obvious to a person having skill in the art at the time the invention was made to employ the fractional step modulo taught by the admitted prior art in the circuit of Petersson et al for the purpose of providing fractional frequency steps and the filter taught by Dekker in the circuit of Petersson for the purpose of removing unwanted high frequency noise.

With regard to claim 4, the variable-rank divider Nb takes the values N1=8 to Np= 24, these values following an arithmetic progression, and wherein the maximum frequency of the synthesizer is given by F4=8x4.68M11Z=37.5M14Z.

With regard to claims 6 and 8, the variable-rank divider (26) takes the values N1=8 to Np= 24.

With regard to claim 7 and 14, wherein 173:=12.5M1-12 is substantially equal to or smaller than a 174=:8/12x37.5M+1Z=25M11Z where a=8/12 is the smallest value obtained in dividing two consecutive elements one after the other.

With regard to claim 9, as understood, the mixer is read on the phase detector (22) of Petersson et al where it receives the output signal (fvco) and a mixing signal (fre).

With regard to claims 5 and 12, although the step frequency F3=12.5MHZ is not equal or slightly lower that (N1/N2)*F4=8/24x37.5MHZ=25MHZ as claimed; however, the step frequency of Petersson et al can be selected by selecting the divisors P and R as shown on Table 1 at column 5. Thus, selecting a predetermined frequency step for the circuit of Petersson in order to accommodate with the requirement of a predetermined system in which the circuit of Petersson is to be used would have been obvious at the time of the invention. The same is true for claims 17-19 and claim 20 in which the reference frequency and the step frequency can be selected to equal to the LCM of the sequence N1.

Response to Applicant's Arguments

The applicant argues that Petersson et al doe not specified how the value Na is related to the value Nb, i.e., "wherein a length of a cycle of evolution of Na is variable and dependent on a value of Nb". The argument is not persuasive because lines 10-36 and Table I in column 5 of Petresson et al clearly shows that the division N is varied from 1000 to 4000 corresponding to the change of the division R from 20 to 60 and the variable-rank divider R is varied according to an arithmetic sequence, 20, 30, 40.

The applicant argues that Petersson do not fairly teach or suggest the claimed fractional step phase-locked loop synthesizer of independent claim 1. The argument is not persuasive because a modified synthesizer of Petersson in view of Dekker (US 6,239,660) would provide a

fractional step phase locked loop synthesizer since the modified synthesizer includes a fractional divider circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DINH T. LE whose telephone number is (571) 272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards, can be reached at (571) 272-1736.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/DINH T. LE/

Primary Examiner, Art Unit 2816